



PTO/SB/08a/b (08-03)

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Substitute for form 1449A/B/PTO				Complete if Known	
				Application Number	10/665,757 (Conf. No. 6828)
				Filing Date	September 19, 2003
				First Named Inventor	Glenn J. Leedy
				Art Unit	2822
				Examiner Name	Pamela E. Perkins
Sheet	1	of	3	Attorney Docket Number	ELM-1 Cont.9

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
TSR		US 4,604,162	08-05-1986	Sobczak	
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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)			
TSR		EP 0 201 380 B1	12-17-1986	Fairchild Semiconductor Corporation	
TSR		EP 0 224 418 B1	06-03-1987	Fujitsu Limited	
TSR		EP 0 419 898 B1	04-03-1991	Siemens Aktiengesellschaft	
TSR		EP 0 455 455 B1	11-06-1991	AT&T Corp.	
TSR		EP 0 487 302 B1	05-27-1992	Shin-ETSU Handotai Company Limited	
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TSR		EP 0 554 063 B1	08-04-1993	Canon Kabushiki Kaisha	
TSR		EP 0 555 252 B1	08-18-1993	Fraunhofer-Gesellschaft Zur Förderung Der Angewandten Forschung E.V.	
TSR		WO 1989 010255	11-02-1989	3D Systems Inc.	
TSR		WO 1990 009093	08-23-1990	Polyolithics Inc.	
TSR		WO 1992 017901	10-15-1992	Integrated System Assemblies Corporation	

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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
<i>PEP</i>		Jones, R.E., Jr. "An evaluation of methods for passivating silicon integrated circuits"; April 1972; pp. 23-8			
		Svechnikov, S.V.; Kobylatskaya, M.F.; Kimarskii, V.I.; Kaufman, A.P.; Kuzovlev, Yu. I.; Cherepov, Ye. I.; Fomin, B.I.; "A switching plate with aluminum membrane crossings of conductors"; 1972			
		Sun, R.C.; Tisone, T.C.; Cruzan, P.D.; "Internal stresses and resistivity of low-voltage sputtered tungsten films (microelectronic cct. conductor)"; March 1973; pp. 1009-16			
		Wade, T.E.; "Low temperature double-exposed polyimide/oxide dielectric for VLSI multilevel metal interconnection"; 1982; pp. 516-19			
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		Boyer, P.K.; Moore, C.A.; Solanki, R.; Ritchie, W.K.; Roche, G.A.; Collins, G.J.; "Laser photolytic deposition of thin films"; 1983; pp. 119-27			
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		Townsend, P.H.; Huggins, R.A.; "Stresses in borophosphosilicate glass films during thermal cycling"; Oct. 21-22, 1986; pp. 134-41			
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		Allen, Mark G.; Senturia, Stephen D.; "Measurement of polyimide interlayer adhesion using microfabricated structures"; 1988; pp. 352-356			
		Chang, E.Y.; Cibuzar, G.T.; Pande, K.P.; "Passivation of GaAs FET's with PECVD silicon nitride films of different stress states"; September 1988; pp. 1412-18			
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		Kochugova, I.V.; Nikolaeva, L.V.; Vakser, N.M., (M.I. Kalinin Leningrad Polytechnic Institute (USSR)); "Electrophysical investigation of thin-layered inorganic coatings"; 1989; pp. 826-828			
<i>DKP</i>		Reche, J.J. H.; "Control of thin film materials properties used in high density multichip interconnect"; April 24-28, 1989; p. 494			

Examiner Signature	<i>Glenn J. Leedy</i>	Date Considered	8/1/00
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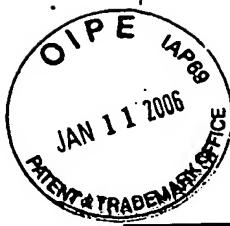
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<i>GLP</i>		Draper, B. L.; Hill, T.A.; "Stress and stress relaxation in integrated circuit metals and dielectrics"; July-Aug. 1991; pp. 1956-62			
<i>GLP</i>		Guckel, H.; "Surface micromachined pressure transducers"; 1991; pp. 133-146			
<i>GLP</i>		Garino, T.J.; Harrington, H. M.; "Residual stress in PZT thin films and its effect on ferroelectric properties"; 1992; pp. 341-7			

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TC		US 3,932,932	01-20-1976	Goodman	
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